Aurora 64b/66b on Polarfire
Reference Design User Guide

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1. REVISION HISTORY

The following table shows the revision history for this document and the associated IP.

Version	Date	Revision
1.0	Jan 2024	Initial Version (for Polarfire)
1.1	April 2024	Fixed a few typos (eg : CRC is supported)

Table 1: Revision history

2. GENERAL INFORMATION

This document describes the content of ALSE Aurora 64B/66B Reference Design for Polarfire.
This design is built for the Polarfire FPGA Evalutation Kit.

The reference design is configured for 1 lane in duplex framing mode, using the SFP+ connector on the board. It is configured to work at 6.25 Gbits/s.

This reference design generates PDU frames, UKB, UFC and NFC. On the RX side, there are checkers for each of these interfaces. The generators follow a known pattern. This way, the design can be used in loopback mode (using a SPF+ loopback module or the internal transceiver loopack) or with two boards connected together.

With this design, we demonstrate the full compliance of our implementation with the Aurora 64b/66b protocol, allowing interoperability with Xilinx FPGAs through Xilinx Aurora 64b/66b IP, as well as with Intel or Lattice boards using our own Aurora IP !

Here is the exact configuration of the IP in the Reference Design. Static parameters can be quickly modified to be adapted to your need !

→ Please let ALSE know if you would like to test our design in a different configuration on this board (different speed, streaming mode…) .

2.1. IP configuration for the Reference Design

In the **current** version, the IP is configured as follow :

- ✓ Full-Duplex.
- ✓ 1 x transceiver lane at 6.25 Gbits/s through SFP+ connector.
- ✓ 64 bits (8 Bytes width) user Datapath.
- ✓ Framing interface (with CRC de-activated).
- ✓ User Flow Control support.
- ✓ User-K blocks support.
- ✓ Native Flow Control support.
- ✓ Clock compensation sequence generation enabled.
- ✓ 156.25 MHz reference clock for transceivers.

Note : we have de-activated the CRC to demonstrate the highest bandwidth achieved.
For some applications, the user can enable the CRC feature to verify automatically the integrity of the data received. If framing mode, activating the CRC while using short frames has a significant impact on the bandwidth.

3.1. Delivery content

Here is the list of file available in the reference design delivery.

aurora_64b66b	Reference folder
└ doc	IP related documentation
└ fit	Synthesis files
└ PolarFire	Binary (.ppd) file only for Polarfire Evaluation Develpment Kit
└ Xilinx_VC707	Project for Xilinx VC707 board (can be adapted for another board)

Figure 1: IP package content

3. ARCHITECTURE

This chapter describes the architecture of the Reference Design provided with the Aurora 64b/66b IP Core.

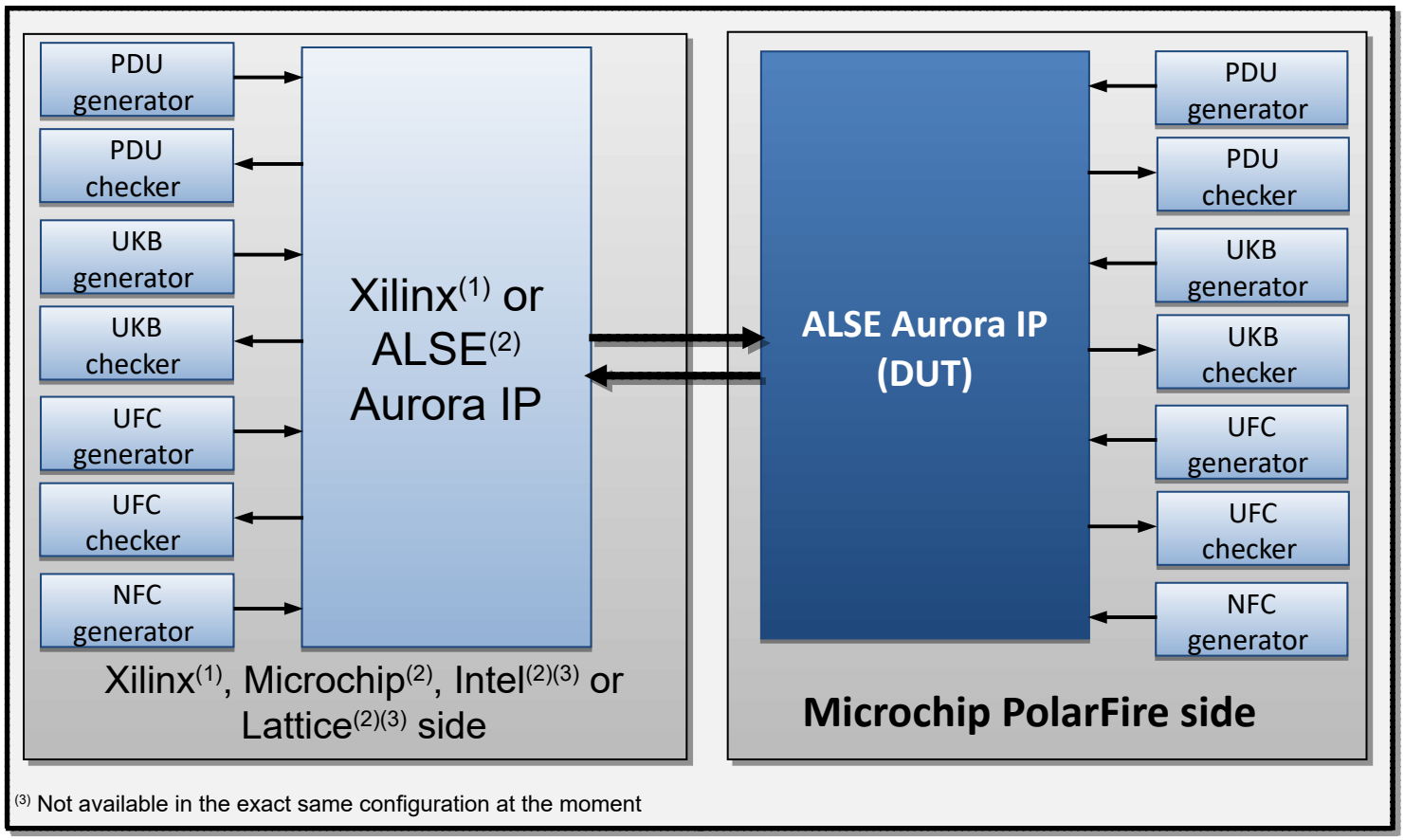

Figure 2: Reference Design architecture

Generator / checker :

The Generator & Checker modules use known pattern sequences for PDU, UFC and NFC control signals. The size change for each frame to test every possibilities. Some pseudo-random IDLEs are inserted inside frames and/or in-between frames.

The data bytes are incremented (counter) as they are valid (using the byte enables), so the checker can easily check for duplicated or lost bytes.

Checking and generation results and control signals are managed through JTAG using in-system probe features (see next section).

3.1. JTAG debugging

Once you programmed the board using Microchip Libero software, you can use the debug tool to monitor the reference design state. Open the *SmartDebug Design* tool to monitor useful signals inside the design : the file "**monitor.txt**" is already at your disposal. Use the load button to add all these probes.

In loopback mode, use this tool. If you have two PolarFire boards, do the same for both sides.
If the board partner is a Xilinx board, you will also need to open the debugging window on Vivado to monitor the generators/checkers states on Xilinx side. While programming the Xilinx FPGA, add the debugging netlist "*.ltx*" and open the VIO (Virtual Input/Output) tool.

JTAG default configuration file allows you to monitor these values :

- Number of PDU frames sent / received.
- Number of UFC frames sent / received.
- Number of Errors in PDU frames received.
- Number of Errors in UFC frames received.
- Number of Errors in UKB frames received.
- Link status signals : link_up, link_tx_ready, link_rx_ready, gxb_ready, block_lock, bonding_ok...

You will also have the control, through JTAG, to reset the design, the aurora or the counters.

3.2. LEDS and buttons

The Polarfire loopback design uses the few control LEDs to output basic debug information.
Most of the debugging and verification is performed from the master board using the JTAG debug features presented above.

- LED4 (F22) : **UFC RX frame counter** is incrementing.
- LED5 (B26) : **PDU RX frame counter** is incrementing.
- LED6 (C26) : **UFC TX frame counter** is incrementing.
- LED7 (D25) : **PDU TX frame counter** is incrementing.
- LED8 (C27) : **Link-up** signal.
- LED9 (F23) : **UKB error** has been detected.
- LED10 (H22) : **UFC error** has been detected.
- LED11 (H21) : **PDU error** has been detected.

LEDs are a faster way to know the state of the reference design but do not replace the JTAG monitor.

Two user buttons are used in this design :

- SWITCH10 (B19) : Main reset of the reference design.
- SWITCH8 (C21) : Counters reset (frame counters and error counters).

4. PICTURES

The picture below shows the Microchip **Polarfire MPF300 evaluation development kit (MPF300-EVAL-KIT)** board in a **x1 configuration** (using SFP+ connectors + optical fiber cable).

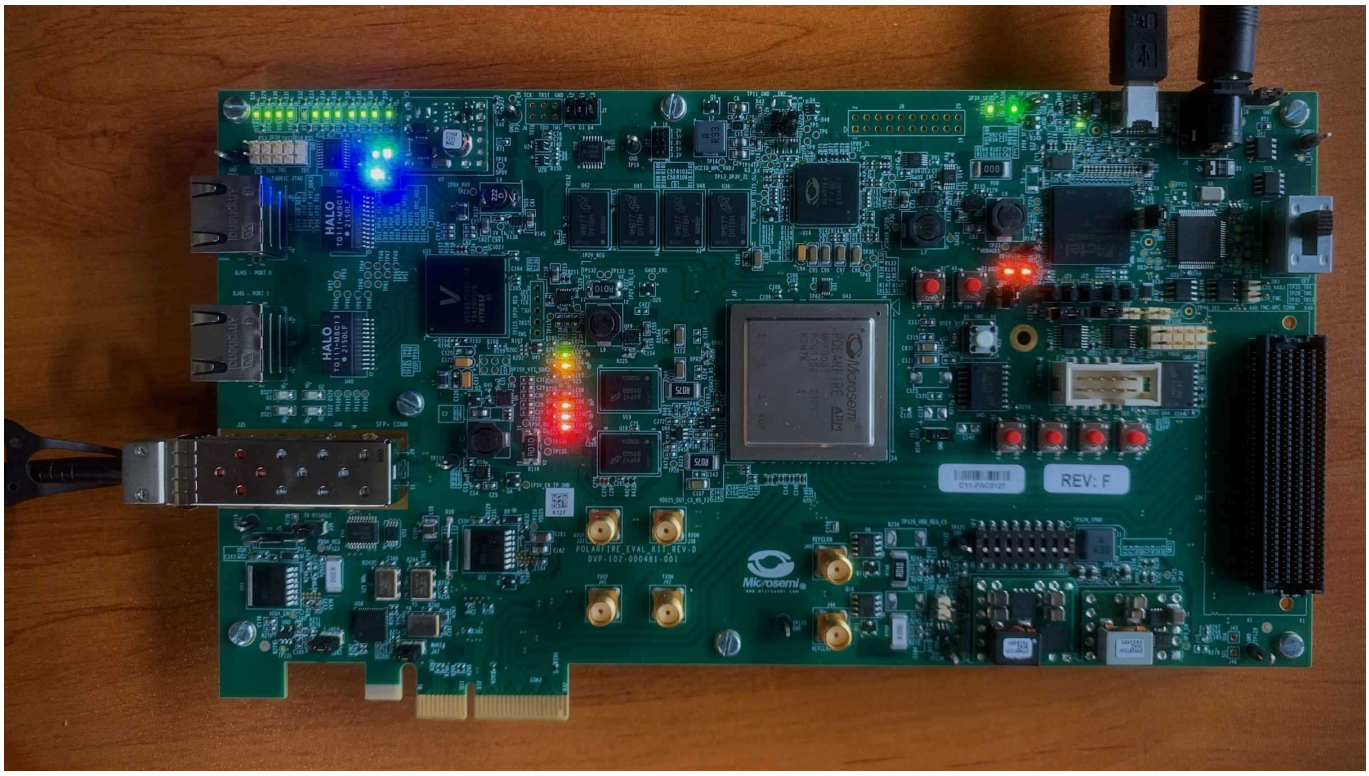

FIGURE 3 : X1 LANE HARDWARE TEST BENCH OVERVIEW

5. TECHNICAL SUPPORT

For any type question about this IP, please contact ALSE Technical Support by **E-mail** at support@alse-fr.com or at a specific E-mail address that you may have received.

If a telephone contact is desired, our R&D office can be reached at +33 1 84 16 32 32, during office hours, CET. You will be either answered directly or directed to an engineer available and competent, depending on the type of question or support. Start by contacting us through e-mail first !

This IP can only be purchased and used after signing the ***ALSE IP License Agreement***.

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